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(54) Nonvolatile semiconductor memory device and the manufacturing method thereof

(57) A nonvolatile semiconductor memory device comprises a first conductive type semiconductor substrate 1, a field oxide film formed on the semiconductor substrate to define an active region, a source region 9a and a drain region 9b which are separated by a channel region near the surface of semiconductor substrate 1 of the active region and diffused with an impurity of the opposite conductive type to the semiconductor substrate 1, a thin gate insulating film 3 formed on the channel region and partially on the source and drain regions 9a and 9b, a first conductive layer 4 formed on the gate insulating film 3 and provided as a floating electrode for accumulating charges, an interlayer insulating film 5 formed on the first conductive layer 4, and a second conductive layer 6 formed on the interlayer insulating film 5 and provided as a control electrode. In the nonvolatile semiconductor memory device, cell characteristics can be greatly improved by thickening the exposed edge of the gate insulating film damaged during fabrication by the re-oxidation process, after the formation of the patterns of the floating gate electrode and the control gate electrode.

FIG. 3

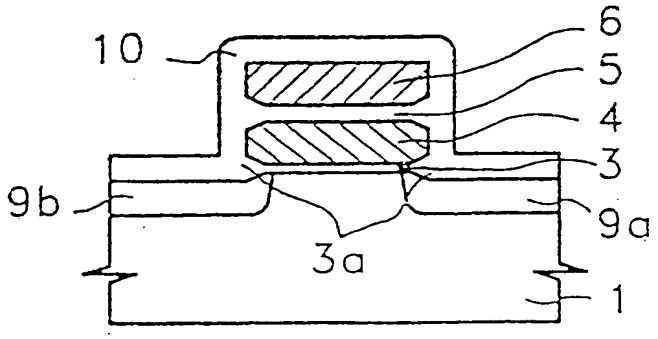

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FIG. 1 (PRIOR ART)

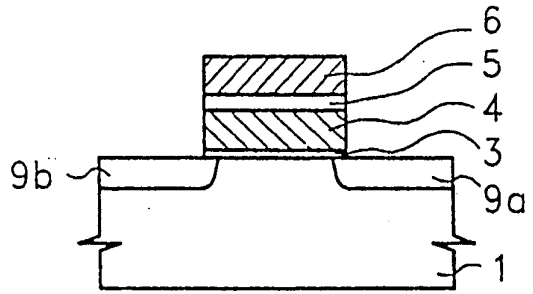


FIG. 2 (PRIOR ART)

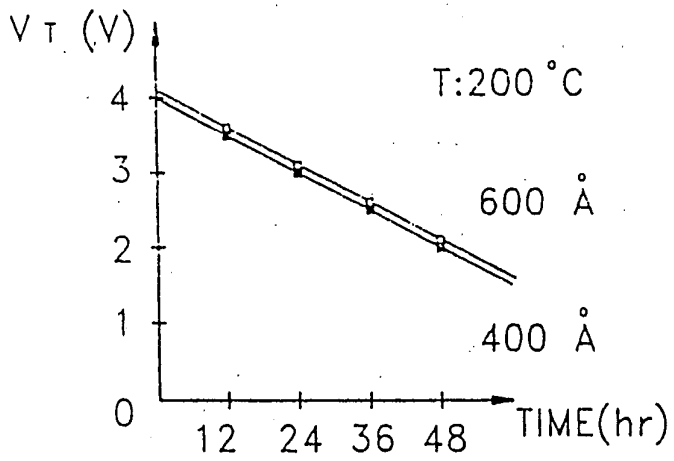


FIG. 3

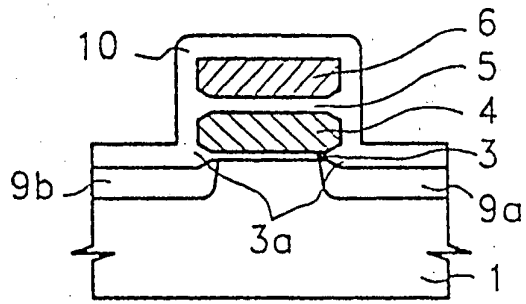


FIG. 4

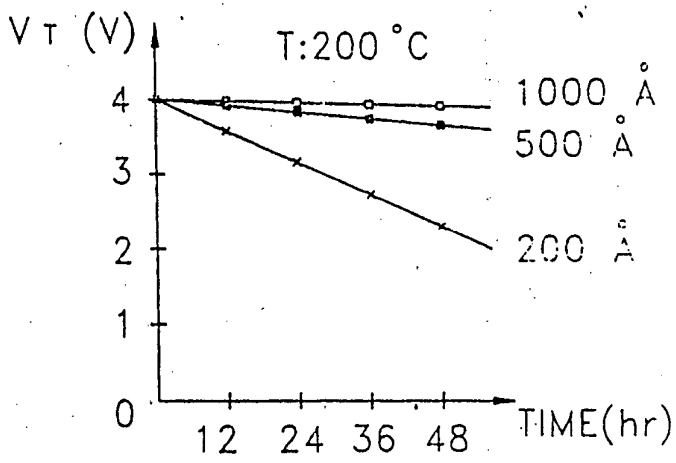


FIG. 5

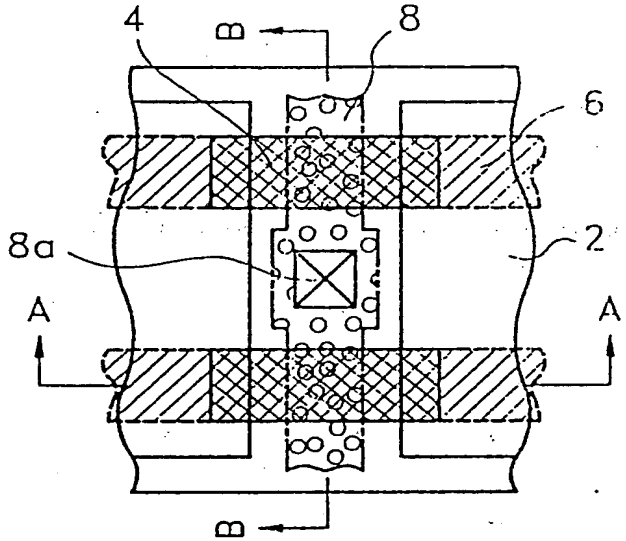


FIG. 6

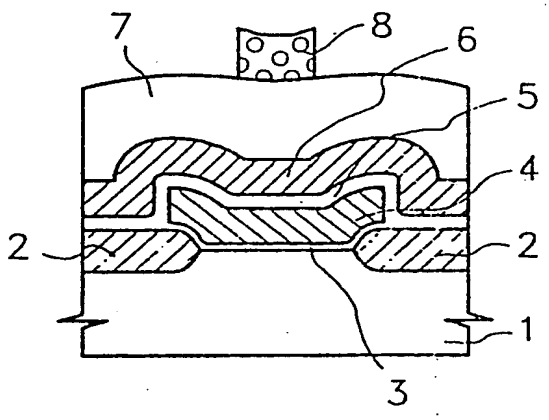


FIG. 7

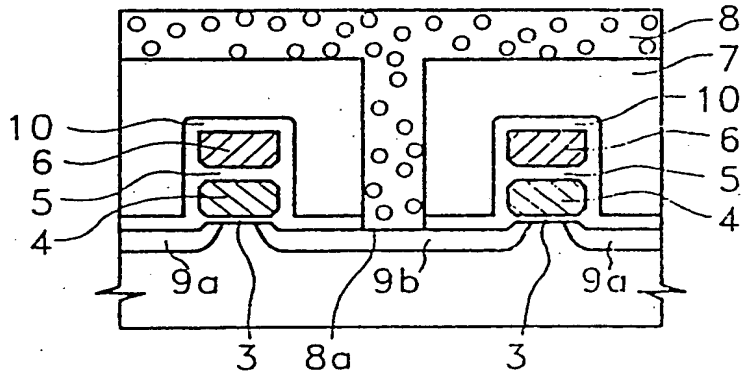


FIG. 8A

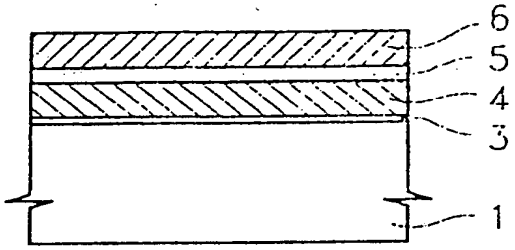


FIG. 8B

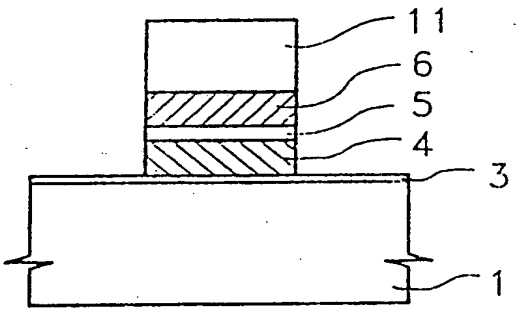


FIG. 8C

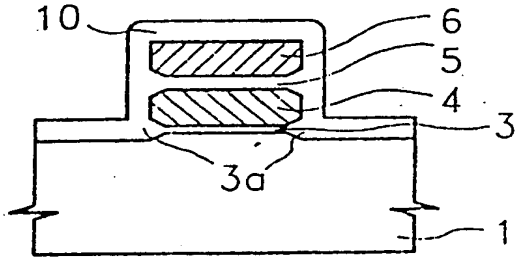


FIG. 8D

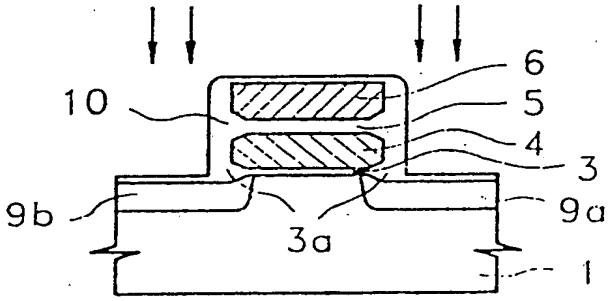


FIG. 9A

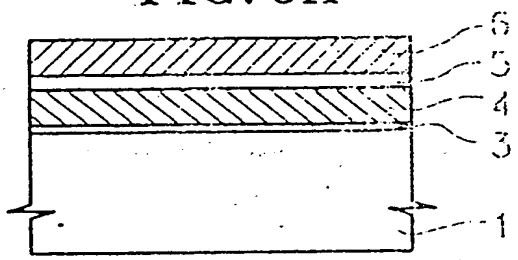


FIG. 9B

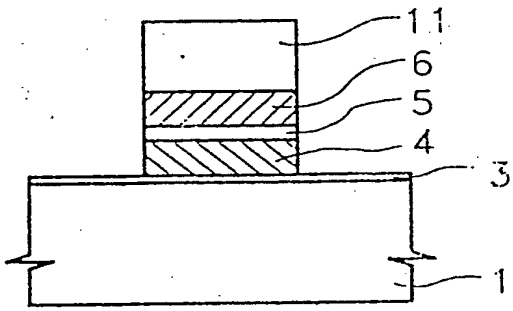


FIG. 9C

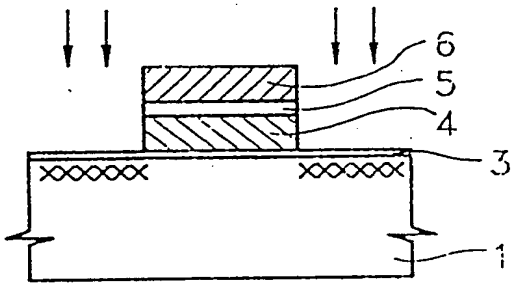
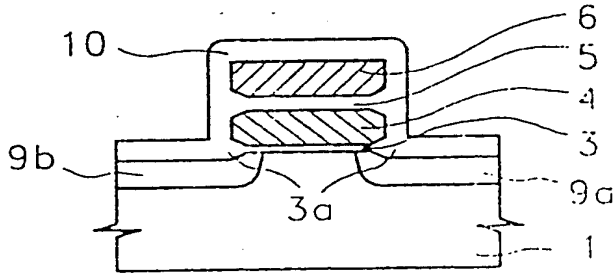


FIG. 9D



NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND THE MANUFACTURING METHOD THEREFOR

The present invention relates to a nonvolatile semiconductor memory device and a manufacturing method therefor, and more particularly, to a nonvolatile semiconductor memory device and a manufacturing method therefor which improves the data retention characteristic.

In general, a nonvolatile semiconductor memory of the floating gate type includes an electrically insulated floating gate electrode underneath the control gate electrode, and charges are induced into the floating gate electrode to be retained as stored information. In the nonvolatile semiconductor memory of the floating gate type, when information is written or erased, a strong electric field is applied to the thin gate oxide film under the floating gate electrode, and charges are injected into or emitted from the floating gate electrode through the thin gate oxide film. Thus, the endurance in the writing and erasing of the information depends on the electric field of the gate oxide film formed under the floating gate electrode.

Such floating gate type nonvolatile semiconductor memories include EPROMs, EEPROMs, flash EEPROMs, etc. FIG.1 of the accompanying drawings shows a cross-sectional view of a conventional semiconductor memory cell structure of the typical floating gate type. In the cell shown in FIG.1, a source region 9a and a drain region 9b, doped with an n^+ impurity near the surface of the p-type silicon substrate 1, are separated from

each other by a channel region. A thin gate oxide film 3 is formed on the channel region and partially on the source region 9a and the drain region 9b. The first conductive layer 4 provided as a floating gate electrode, the insulating film 5, and the second conductive layer 6 provided as a control gate electrode are formed on the gate oxide film 3. To write information in an EPROM having such a cell structure, high voltages of 12.5 V and 7 to 8 V are respectively supplied to the control gate electrode and the drain region, thereby generating an electric field in the floating gate electrode and accelerating electrons in the pinch-off region on the drain region side and causing them to be injected into the floating gate electrode. When an ultraviolet ray is irradiated to erase the information, the injected electrons are emitted to initialize the memory cell. However, in a EEPROM, if a high voltage (about +20V) is supplied to a control gate electrode with the drain grounded, electrons are injected into the floating gate electrode through a thin gate oxide film. Conversely, if the voltage is supplied to the drain with the control gate electrode grounded, electrons are emitted through the thin gate oxide film from the floating gate electrode. As described above, the injection and the emission of the electrons are carried out through the gate oxide film, resulting in the variation of the threshold voltage in the channel region, and thus obtaining the nonvolatile information memory function.

In the conventional nonvolatile semiconductor memory of the floating gate type, since the injection and the emission

of the electrons are carried out by the hot electron or the tunnelling effect, a thin gate oxide film should be formed to effectively carry out the injection and the emission of the electrons. Conventionally, an EPROM has a thickness of approximately 300 Å and a EEPROM has a thickness of 100 Å.

In such conventional nonvolatile semiconductor memories of the floating gate type, the electrons injected into the floating gate electrode when writing information are enclosed by the potential barrier resulting from the surrounding insulating film, hence stored. However, if the surrounding insulating film is damaged during the fabrication process or has a defect, the injected electrons leak through the damaged or defected portion. Electron leakage from the floating gate electrode deteriorates the reliability of the memory device.

To find out the main reason of the electron leakage, the information is stored in two samples having interlayer insulating film thicknesses of 400 Å and 600 Å. Then the samples are baked for 48 hours at 200 ° C. The variation in threshold voltage Vt is checked at 12 hour intervals and the result is obtained as a graphic diagram shown in FIG.2 of the accompanying drawings showing that regardless of interlayer insulating film thickness, the initial threshold voltages Vt of both samples decrease from +4V to approximately +2V over 48 hours. Therefore, the electron leakage of the floating gate electrode is not related to the thickness of the interlayer insulating film, and mainly occurs through the thin gate oxide film.

In the conventional cell structure shown in FIG.1, a thin gate oxide film 3, a first conductive layer 4, an interlayer insulating film 5, and a second conductive layer 6 are sequentially stacked on a silicon substrate 1, and the second conductive layer 6, the interlayer insulating film 5, and the first conductive layer 4 are sequentially etched to form a stacked floating gate electrode and control gate electrode. At this time, if the etching is excessive, the edges of the gate oxide film 3 under the floating gate electrode 4 are also etched somewhat, or the exposed edges of the gate oxide film 3 receive an impulse and are then damaged by the responsive ions during reactive ion etching. Accordingly, the exposed edges of the gate oxide film 3 are damaged during the fabrication process, which causes the majority of electron leakage.

Specifically, in the case of flash EEPROMs, gate oxide film is about 100 Å thick, and in highly integrated devices, in the megabit region or more, the thickness of the insulating film is further decreased, so it is highly desirable to solve the problem of the data loss by electron leakage.

It is an object of the present invention to provide a nonvolatile semiconductor memory device which can improve the data retention property by improving a gate oxide film, to solve the above problems.

It is another object of the present invention to provide the most suitable method for manufacturing the nonvolatile semiconductor memory device.

According to the present invention there is provided

a nonvolatile semiconductor memory device which comprises:

a semiconductor substrate of a first conductive type;

a field oxide film formed to define an active region on the semiconductor substrate;

a source region and a drain region, separated from each other by the channel region, near the surface of the semiconductor substrate of the active region and diffused with impurities of the opposite conductive type to the semiconductor substrate;

a thin gate insulating film formed on the channel region, part of source region and part of drain region;

a first conductive layer formed on the gate insulating film and provided as a floating electrode for accumulating charges;

an interlayer insulating film formed on the first conductive layer; and

a second conductive layer formed on the interlayer insulating film and provided as a control electrode,

wherein the thickness of the edge of the thin gate insulating film is thicker than that of portions other than the edge.

Thus, since the edge of the gate oxide film is formed as a thick film, preventing electron leakage, and improving the data retention property.

According to another aspect of the present invention there is provided a manufacturing method for a semiconductor memory device which comprises the steps of:

forming a field oxide film to define an active region

on a first conductive type semiconductor substrate;

thermally growing a thin gate oxide film on the surface of the semiconductor substrate of the active region;

depositing a first polycrystalline silicon doped with the impurity on the thin gate oxide film to form a pattern of the first polycrystalline silicon deposited by a conventional photolithography process;

covering the first patterned polycrystalline silicon layer with an interlayer insulating film;

forming a pattern of a first polycrystalline silicon layer provided as a floating electrode for accumulating charges and a pattern of an impurity-doped second polycrystalline silicon layer overlapping the floating electrode and provided as a control electrode by depositing the second polycrystalline silicon layer on the interlayer insulating film and sequentially etching the stacked layers of the second polycrystalline silicon layer, the interlayer insulating film, and the first polycrystalline silicon layer;

growing a thermal oxide film having a thickness at least two times as thick as that of the thin gate oxide film on the whole surface of the resultant, after the step of forming the patterns;

thinly forming the thickness of the thermal oxide film formed on the surface of the active region by etching the thermal oxide film by an anisotropically etching process, after the step of growing the thermal oxide film; and

implanting the ions of the impurity having the opposite conductive type of the substrate and then forming a

source region and a drain region,

whereby the edge of the thin gate oxide film is thickly formed by the bird's beak extending toward the active region from the thermal oxide film.

Also, in the above-described manufacturing method, the step of ion-implantation can be carried out first, and then the growth of the thermal oxide film can be carried out later.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

FIG.1 is a cross-sectional view of the conventional stacked type flash EEPROM cell;

FIG.2 is a graphical representation showing the characteristic variation of time versus the threshold voltage Vt according to the oxide film thickness of the interlayer gate of the conventional stacked type flash EEPROM cell;

FIG.3 is a cross-sectional view of a stacked type flash EEPROM cell according to an embodiment of the present invention;

FIG.4 is a graphical representation of the characteristic variation of time versus threshold voltage Vt according to the thermal oxide thickness of the stacked type flash EEPROM cell of embodiments according to the present invention at 200 ° C;

FIG.5 is a planar layout diagram of a stacked type flash EEPROM cell array according to an embodiment of the present invention;

FIG.6 is a cross-sectional view taken on line A-A of

FIG.5;

FIG.7 is a cross-sectional view taken on line B-B of FIG.5;

FIGs. 8A to 8D are cross-sectional views showing an embodiment of a fabrication process sequence of the stacked type flash EEPROM according to an embodiment of the present invention; and

FIGs.9A to 9D are cross-sectional views showing a another preferred embodiment of the fabrication process sequence according to the present invention of the stacked type flash EEPROM.

Referring to FIG.3, in a cell structure of a floating gate type nonvolatile semiconductor memory device according to an embodiment of the present invention, a source region 9a doped with n^+
impurities and a drain region 9b on a p-type semiconductor substrate 1 are formed by being separated by a channel region, a gate insulating film 3, for instance, by an oxide film of approximately 100 Å, is formed over the channel region, part of source region 9a, and part of drain region 9b and a first conductive layer 4 for a floating gate electrode, the interlayer insulating film 5 and a second conductive layer 6 for a control gate electrode are formed by being stacked on a gate insulating film 3, whereby the cell is formed by depositing a thermal oxide film 10 to be at least two times thicker than the gate insulating film 3 on the surface of the above structure. When the thermal oxide film 10 is grown, the bird's beak extending toward and connecting to the active

region of the gate insulating film 3, from the thermal oxide film, is provided as a thick film 3a of the gate insulating film 3. Thus, even if the exposed edge part of the gate insulating film 3 is damaged, the formation of the thick film 3a compensates it, thereby preventing electron leakage.

Referring to FIG.4, to test the cell structure reliability for samples having thickness of 200 Å, 500 Å, and 1,000 Å as the thermal oxide film 10, a high voltage of +20V is supplied to the second conductive layers 6, and then the source regions 9a, the drain regions 9b, and the substrates 1 are grounded. Electrons are injected into the first conductive layers 4, e.g., the floating gate electrodes for 100mS. Then, the samples are baked in a furnace at 200° C for 48 hours. The threshold voltage Vt of each sample is measured every 12 hours and the graphic diagram obtained is shown in FIG.4, showing that when the thermal oxide film of 200 Å is formed, the decreasing characteristic of the threshold voltage is similar to the conventional cell structure represented. However, in cases of the 500 Å and 1,000 Å samples, it is shown that the decrease in threshold voltage is remarkably reduced. As for the 1,000 Å sample, a threshold voltage nearly that of the initial state is maintained even after 48 hours.

Now, the manufacturing method of the above-described embodiments of the present invention will be disclosed.

FIG.5 is a planar lay-out diagram of a nonvolatile semiconductor memory device according to an embodiment of the present invention, FIG.6 is a sectional view taken on line A-A of FIG.5, and FIG.7 is a sectional view taken on line B-B of

FIG.5. In these drawings, the corresponding cell structure elements use the same reference numerals as their like elements shown in FIG.3. The numeral 2 in FIG.5 indicates a field oxide film formed on an isolation region in the sectional view of FIG.6. In FIGs.6 and 7, the numeral 7 indicates a surface protecting layer for planarizing the surfaces such as a BPSG film, a SOG film, etc., and the numeral 8 indicates a metallic electrode provided as a bit line which contacts the drain region 9b through the contact hole 8a.

With reference to FIG.8A to FIG.8D, a preferred embodiment of a manufacturing method of a nonvolatile semiconductor memory according to an embodiment of the present invention will be described.

First of all, to form a transistor in a region of a peripheral circuit part of a p-type silicon wafer substrate 1 using a CMOS technique, a pad oxide film is grown, and the part of the pad oxide film corresponding to n-well region is then etched and removed. Successively, p^+ ions of an n-type impurity are injected into the portion in which a pad oxide film has been removed, with a density of 4.5E12 ions/cm^2 at an energy level of 150 KeV, and are heated for 10 hours at 1,100 °C to activate the impurity to form an n-well. The pad oxide film is completely removed and the pad oxide film is grown to be a thickness of 380 Å, on which the nitride film of 1,500 Å is deposited. The part corresponding to the isolation region of the nitride film is removed by a dry method and the photoresist is covered on the n-well region. Successively, with the nitride film and the photoresist film as a mask, the boric acid ions

of p-type impurity are injected with a density of 5.0E13 ions/cm^2 at 30 KeV, and the photoresist is removed, and the field oxide film is grown to be a thickness of approximately 8,000 Å. Successively, the nitride film and the pad oxide film are completely removed. The gate oxide film of approximately 300 Å is formed in the active region, and the boron ions are injected with 5.0E11 ions/cm^2 at 30 KeV to control the threshold voltage of the transistor in the active region of the peripheral circuit part. After the boron ions are injected with 2.0E12 ions/cm^2 at 30 KeV energy to control the cell threshold voltage in the active region of the memory cell part, the gate oxide film is removed and the thin gate insulating film 3 is grown to be an oxide film of 100 Å. After that, the first polycrystalline silicon, provided as a floating gate electrode of the memory cell part and the transistor gate electrode of the peripheral circuit part, is deposited to be a thickness of 2,000 Å using an LPCVD method. Successively, to reduce the resistance of the deposited polycrystalline silicon, $POCl_3$ is used to dope the impurity. Successively, the first polycrystalline silicon layer is patterned using a conventional photolithography process. Then, the first polycrystalline silicon layer of the memory cell part is covered with an interlayer insulating film 5 such as an O/N/O film. After the first oxide film of the O/N/O film is deposited to be a thickness of 160 Å and the nitride film is deposited to be a thickness of 200 Å, the second oxide film is processed at 1,000 °C for ten minutes in a wet oxygen O_2 atmosphere to form a thermal oxide film of 40 Å which is a thickness of oxide film

grown on the nitride film. Then, to form the gate of the peripheral circuit, the peripheral circuit is defined by a photoresist process, and then the O/N/O film of the peripheral circuit is removed by the etching process, and then the gate oxide film is grown to be 400 Å. At this time, the growth of oxide film is restrained in the region covered with the O/N/O film. Successively, to provide the control gate electrode of the memory cell part and the polystructure of the peripheral circuit part, the second polycrystalline silicon is deposited to be a thickness of 4,000 Å and the impurity is doped by applying $POCl_3$ in the second polycrystalline silicon layer to decrease its resistance. Accordingly, the memory cell part obtains a structure having the cross-section shown in FIG.8A. To further decrease the resistance of the second polycrystalline silicon layer, a silicide film having a high melting point such as tungsten can be stacked.

After the above process, the polycrystalline silicon pattern of the peripheral circuit part is formed, and a pattern is formed in the memory cell part with the photoresist 11 by a conventional photolithography process. The second polycrystalline silicon layer, the interlayer insulating film of an O/N/O structure, and the first polycrystalline silicon layer are sequentially etched with the pattern of the photoresist 11 as a mask, completing the memory cell. FIG.8B shows a cross-sectional view of the stacked structure of the second conductive layer 6 for a control gate electrode, the interlayer insulating film 5, and the first conductive layer 4 for a floating gate electrode, obtained by the etching

process.

Then, the resultant is placed in a furnace and processed for 15 minutes in a wet oxygen O_2 atmosphere to grow a thermal oxide film 10 to 1,000 Å on the whole surface. Accordingly, the bird's beak extending toward the edges of the gate insulating film 3 from the thermal oxide film 10 provides a thick film 3a around the edge of the floating gate 3 as shown in FIG.8C.

Successively, the 1,000 Å thermal oxide film 10 is anisotropically etched by a responsive ion etching method to remove approximately 600 Å of the oxide film, thinning the portion of the thermal oxide film 10 on which the source region and the drain region will be formed. Then, the arsenic ions of the n^+ type impurity are injected with a density of 6.0E15 ions/cm^2 at 150 KeV through the thinned oxide film. A heating process is then carried out for 20 minutes at 975 ° C, forming the n^+ source region 9a and n^+ drain region 9b near the surface of substrate 1 as shown in FIG.8D. Thus, the cell structure according to the present invention is obtained.

After that, to form a source and a drain of a transistor in the n-well region of the peripheral circuit part, boron ions are injected with a density of 2.0E15 ions/cm^2 at 40 KeV, and a LTO film of the 1,700 Å and a BPSG film of 7,000 Å on the whole surface are sequentially etched. The BPSG film is then reflowed for 30 minutes in an N_2 atmosphere to roughly planarize the surface, forming the surface protecting layer 7.

Afterwards, the metal contact hole is formed. A pattern of 1 μm-thick metal is deposited, completing the metal

wiring. After that, the contact between the metal in the contact hole and the active region forms an ohmic contact through an alloy process.

FIG. 9A to FIG.9D are cross-sectional views showing another embodiment of the fabrication method of a nonvolatile semiconductor memory device having a cell structure according to the present invention. The process shown in FIGs.9A and 9B are identical with that of FIGs. 8A and 8B described above.

In the second preferred embodiment according to FIG.9C, the stacked structure of the first conductive layer 4, the interlayer insulating film 5, and the second conductive layer 6 is formed, and arsenic ions are injected with a density of 6.0E15 ions/cm^2 at 75 KeV through the thin gate insulating film 3.

Referring to FIG.9D, after the injection process, a wet O_2 atmosphere is applied at 975 ° C for 7 minutes, and then a dry atmosphere is applied for 23 minutes, thereby growing the thermal oxide film 10 to be approximately 1,000 Å. During the growth process of the thermal oxide film, the impurity ions injected near the surface of the substrate 1 are activated, forming the n^+ source region 9a and the n^+ drain region 9b.

As compared with the embodiments illustrated in FIGs 8A to 8D that illustrated in FIGs 9A to 9D carries out the ion injection process first and the thermal oxide film growth process later, benefitting economically by omitting the ion etching process, the drive-in process for activating the injected ions, etc. Also, the ion-injection energy level can be halved.

Embodiments of the present invention as described above prevent the leakage of electrons stored in the floating gate electrode due to environmental conditions such as noise, high temperature, humidity, and pressure, improving the data retention property. That is, in the nonvolatile semiconductor memory device, a pattern of the floating gate electrode and a pattern of control gate electrode are formed, and the exposed edge of the active region of gate insulating film damaged in the fabrication process is thickened, greatly improving cell characteristics. Thus providing a nonvolatile semiconductor memory device of high reliability.

CLAIMS:

1. A nonvolatile semiconductor device comprising:

a semiconductor substrate of a first conductive type;

a field oxide film on said semiconductor substrate to define an active region;

a source region and a drain region which are separated by a channel region near the surface of the semiconductor substrate of said active region, and diffused with an impurity of the opposite conductive type to said semiconductor substrate;

a thin gate insulating film on said channel region and on part of said source region and part of said drain region;

a first conductive layer on said gate insulating film and provided as a floating electrode for accumulating charges;

an interlayer insulating film on said first conductive layer; and

a second conductive layer on said interlayer insulating film and provided as a control electrode,

wherein the thickness of the edge of said thin gate insulating film is thicker than that of portions other than said edge.

2. A nonvolatile semiconductor device as claimed in claim 1, wherein the thickness of the thick portion of said thin gate insulating film is at least two times that of the thinner portion.

3. A nonvolatile semiconductor device substantially as herein described with reference to FIG 3 with or without reference to any of FIGs 4 to 9D of the accompanying drawings.

4. A method for manufacturing a nonvolatile semiconductor memory device comprising the steps of:

forming a field oxide film to define an active region on a semiconductor substrate of a first conductive type;

thermally growing a thin gate oxide film on the surface of the semiconductor substrate of said active region;

depositing a first polycrystalline silicon layer doped with impurities and forming a pattern of a first deposited polycrystalline silicon layer by a conventional photolithography process;

covering said first patterned polycrystalline silicon layer with an interlayer insulating film;

forming a pattern of a first polycrystalline silicon layer provided as a floating electrode for accumulating charges and a pattern of an impurity-doped second polycrystalline silicon layer provided as a control electrode overlapping said floating electrode, and depositing said second polycrystalline silicon layer on said interlayer insulating film, and using a conventional photolithography process to sequentially etching the stacked layers of the second polycrystalline silicon layer, the interlayer insulating film, and the first polycrystalline silicon layer;

growing a thick thermal oxide film at least two times as thick as that of said thin gate oxide film on the whole

surface of the resultant, after the step of forming said patterns;

thinly forming a film thickness of a thermal oxide film formed on the surface of said active region by etching said thermal oxide film by an anisotropically etching process, after the step of growing said thermal oxide film; and

forming a source region and a drain region by ion-implanting impurities of the opposite conductive type to the substrate near the surface of the semiconductor substrate of the active region through said thinned thermal oxide film and then activating the injected impurities,

whereby the thick portion of said thin gate oxide film is formed by a bird's beak extending toward said thin gate oxide film from said thermal oxide film.

5. A method for manufacturing a nonvolatile semiconductor memory device as claimed in claim 4, wherein in the step of growing said thermal oxide film, a wet oxide oxygen atmosphere is held for approximately 15 minutes, thereby growing the thermal oxide film to a thickness of approximately 1,000 Å.

6. A method for manufacturing a nonvolatile semiconductor memory device as claimed in claim 4 or 5, wherein said interlayer film is formed as an oxide film, a nitride film, or a stacked film of oxide and nitride.

7. A method for manufacturing a nonvolatile

semiconductor memory device comprising the steps of:

forming a field oxide film for defining an active region on a first conductive type semiconductor substrate;

thermally growing a thin gate oxide film on the semiconductor substrate of said active region;

depositing a first polycrystalline silicon layer doped with an impurity on said thin gate oxide film and forming a pattern by a photolithography process;

covering said first patterned polycrystalline silicon layer with an interlayer insulating film;

forming a pattern of a first polycrystalline silicon layer provided as a floating electrode for accumulating charges and a pattern of an impurity-doped second polycrystalline silicon layer provided as a control electrode overlapping said floating electrode by depositing said second polycrystalline silicon on said interlayer insulating film and using a photolithography process to sequentially etching the stacked layers of the second polycrystalline silicon layer, the interlayer insulating film and the first polycrystalline silicon layer;

ion-implanting an impurity of the opposite conductive type to the substrate near the surface of the semiconductor substrate of said active region, after the step of forming said patterns; and

growing a thick thermal oxide film at least two times as thick as that of said thin gate oxide film on the whole surface of the resultant, after the step of said ion-implantation,

wherein the edge of said thin gate oxide film is thickly formed by a bird's beak extending from said thermal oxide film toward said thin gate oxide film.

8. A method for manufacturing a nonvolatile semiconductor memory device as claimed in claim 7, wherein the step of growing said thermal oxide film is processed approximately seven minutes in a wet oxygen atmosphere at approximately 975 ° C, and is then processed approximately 23 minutes in a dry oxygen atmosphere, thereby growing a thermal oxide film to a thickness of approximately 1,000 Å.

9. A method for manufacturing a nonvolatile semiconductor memory device substantially as hereinbefore described with reference to FIG. 3 of the accompanying drawings.

10. A method of manufacturing a nonvolatile semiconductor memory device substantially as hereinbefore described with reference to FIG 3 with reference to any of FIGs 4 to 9D of the accompanying drawings.

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Relevant Technical fields

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Search Examiner

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Databases (see over)

(i) UK Patent Office

(ii)

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Documents considered relevant following a search in respect of claims 1-10

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	US 4892840 (TEXAS INSTR) see Figures 5, 7	1,4,7
X	US 4519849 A (INTEL) see column 3 lines 3-36	1,4,7
X,&	US 4412310 A (INTEL) see Figure 2	1,4,7
X,&	GB 2085226 A (INTEL) see Figure 2 and page 2 lines 49-49	1,4,7

Category	Identity of document and relevant passages	Relevant to claim(s)

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X: Document indicating lack of novelty or of inventive step.

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